MODULATION KIT

Modulation Kit

The modulation kit consists of three sections: a signal source, a modulator, and a demodulator. The front panel controls to each of these sections are shown in Figures 1-3. The following sections explain the pertinent features of the modulation kit:

Synchronised Signals on Signal Source Board

The signal source allows the generation of both sinusoidal and digital signals. These signals with the exception of a 10 KHz signal are all synchronised with a 1 MHz clock. Such synchronisation allows the various signals generated in the modulator to be clearly displayed on an oscilloscope. The digital signals are unipolar (0 to 5 V) and can be converted to polar signals (-2.5 to 2.5 V) via the circuitry labelled "unipolar to polar".

PRN Generator

The PRN (pseudo random noise) generator generates a pseudo random binary sequence of 0-5V NRZ unipolar pulses. The sequence length is 2¹⁵-1 pulses.

Frequency Feedback on FM Modulator

The frequency feedback network in the modulator board requires explanation. This network provides feedback to the input of the VCO so that its unmodulated frequency (100 kHz) is synchronised with the 1 MHz clock and hence the modulating signals available on the signal source board. This allows FM and FSK signals to be clearly displayed on an oscilloscope. The feedback network is lowpass with a bandwidth of less than 1 Hz and is such that it does not affect the generation of FM or FSK signals provided the frequency of the modulating signals is greater than around 100 Hz. A LED indicates when the frequency feedback network has synchronised the unmodulated output frequency of the VCO with the 1 MHz clock. If the VCO is modulated with a unipolar signal the frequency feedback network will not achieve lock.

Modulator Board

The modulator can generate, in addition to AM, DSB, SSB, QAM, and FM signals, binary ASK (amplitude shift keyed), FSK (frequency shift keyed), and PSK (phase shift keyed) signals.

Demodulator Board

The demodulator is based on extracting a synchronised signal via a Phase Locked Loop (PLL) (either a standard PLL or a COSTAS PLL) and synchronous detection.

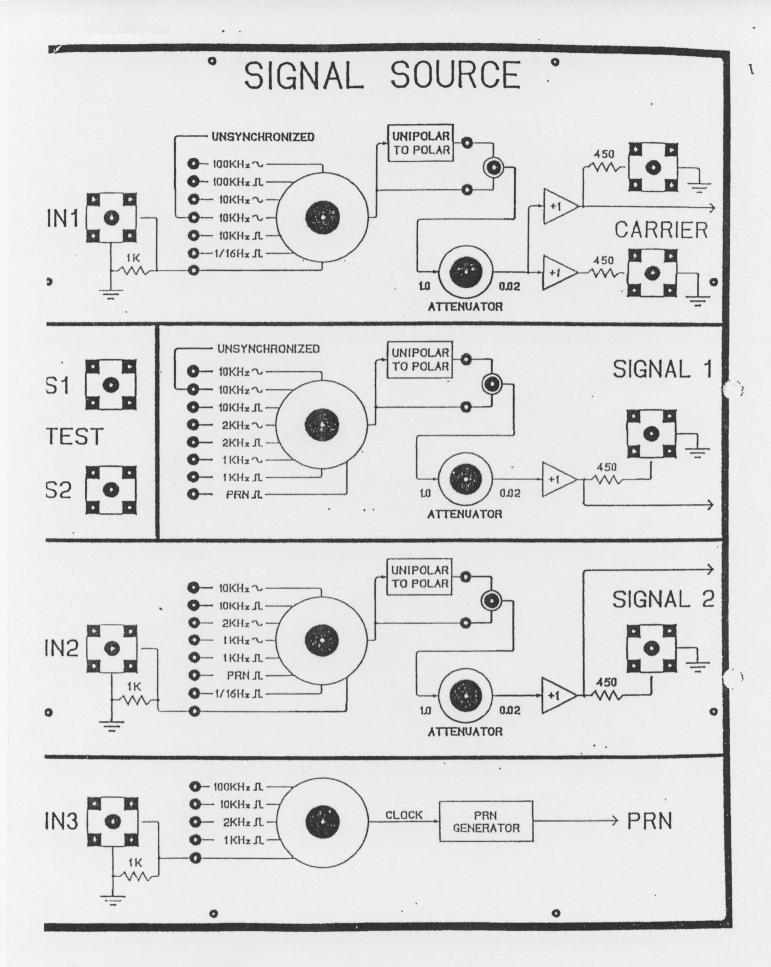


Figure 1

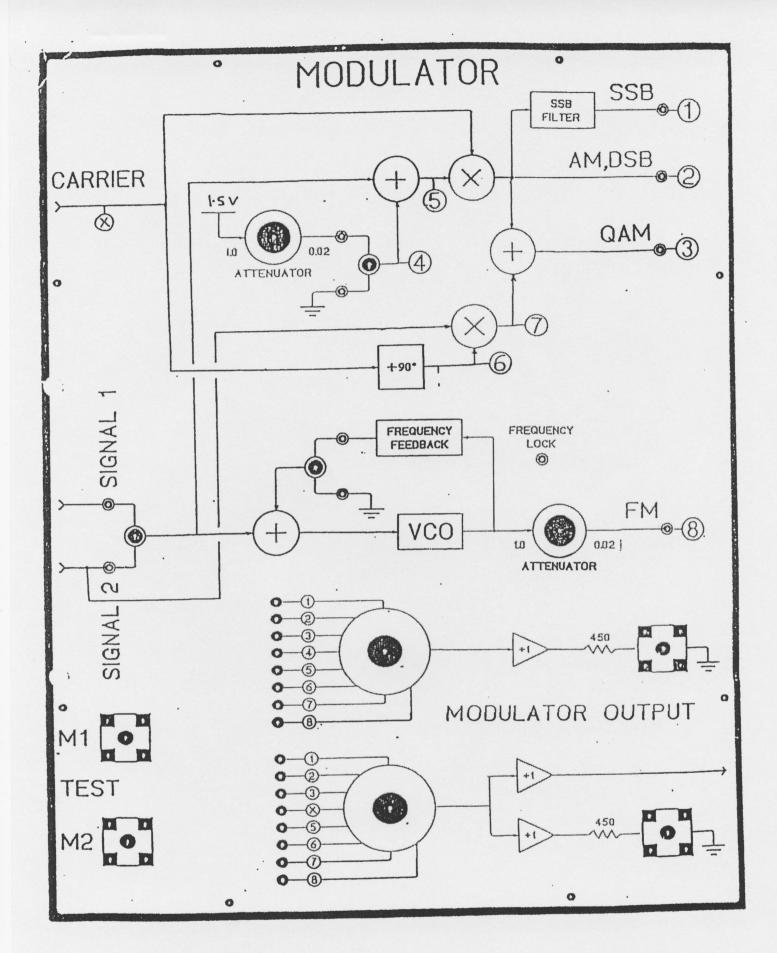


Figure 2

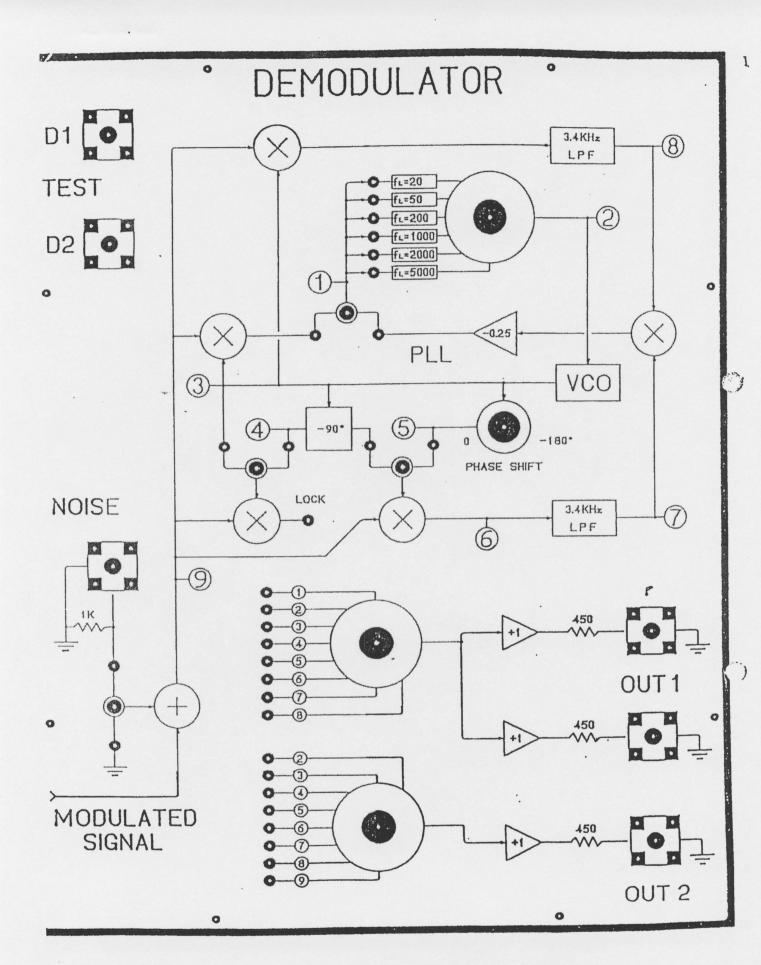


Figure 3