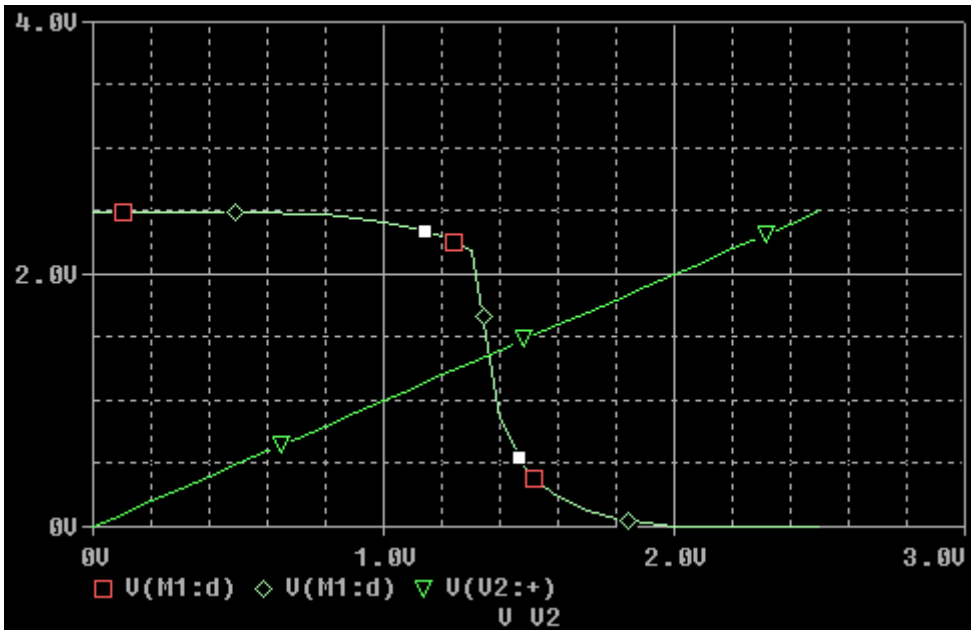
Lab 2 Report

By Lyndon White 20 361 362

Results

B) Find V_{IH} , V_{IL} , V_M for $\frac{W_p}{W_n}=2$



for V_{IH} , V_{IL} slope =-1.

Eyeballing the Graph, and using the cursor: $V_{IL}=1.30\text{V}$, $V_{IH}=1.48$.

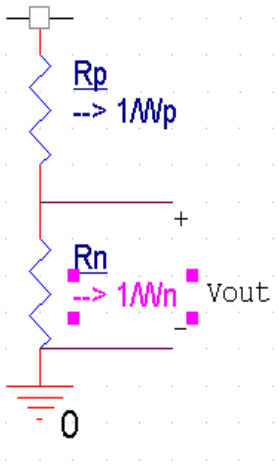
V_M is the point where $V_{i.n}=V_{out}$,

to find this a Plot of $V_2=V_{in}$ was added., Where this intersects the curve

$V_{out}=V_{in}=V_m=1.38\text{V}$

C Investigate relationship between Wp/Wn and Vm

Wp/Wn	Vm (volts)
1/4=0.25	0.966
1/2=0.5	1.110
1/1=1	1.258
3/2=1.5	1.335
2/1=2	1.400
4/1=4	1.530



We see that as the PMOS becomes wider compared to the NMOS the Vm increases.
At Vm both the PMOS and Nmos are in saturation, they are acting as resistors.

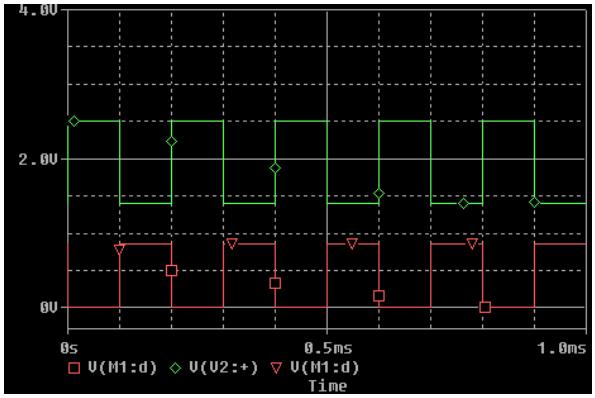
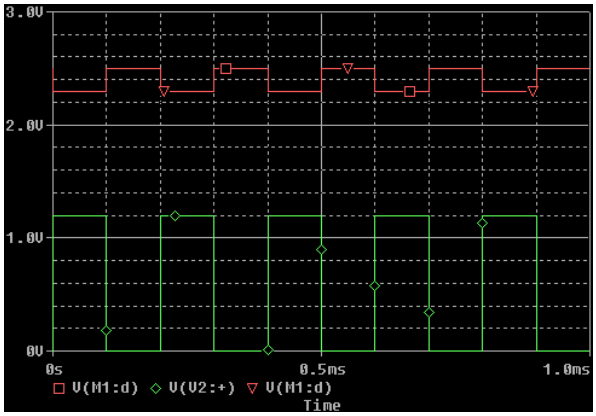
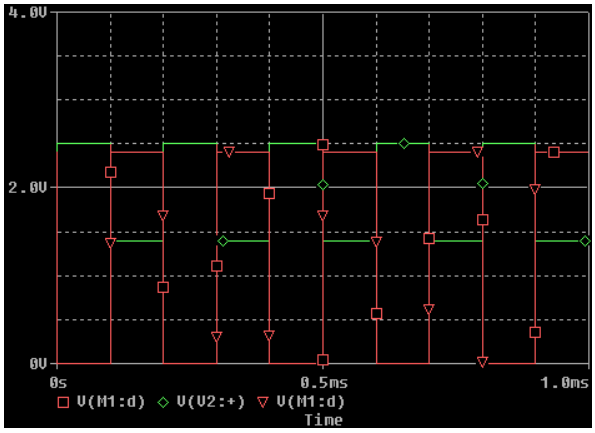
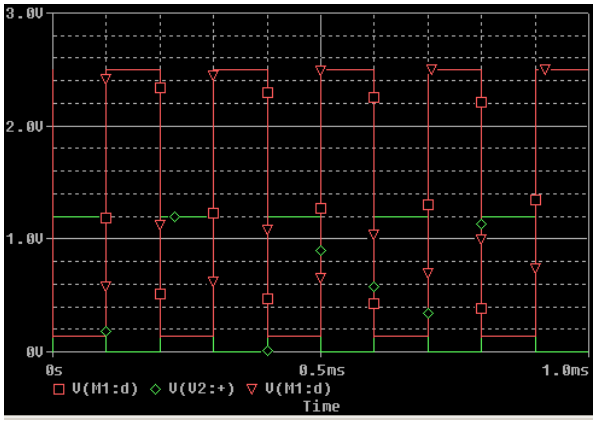
Thus we have a voltage divider. $$V_m = \frac{R_n}{(R_n + R_p)} \propto \frac{1/W_n}{(1/W_n + 1/W_p)} \propto \frac{W_p}{(W_n + W_p)}$$

Ie the wider the PMOS compared to the NMOS the higher the Vm.

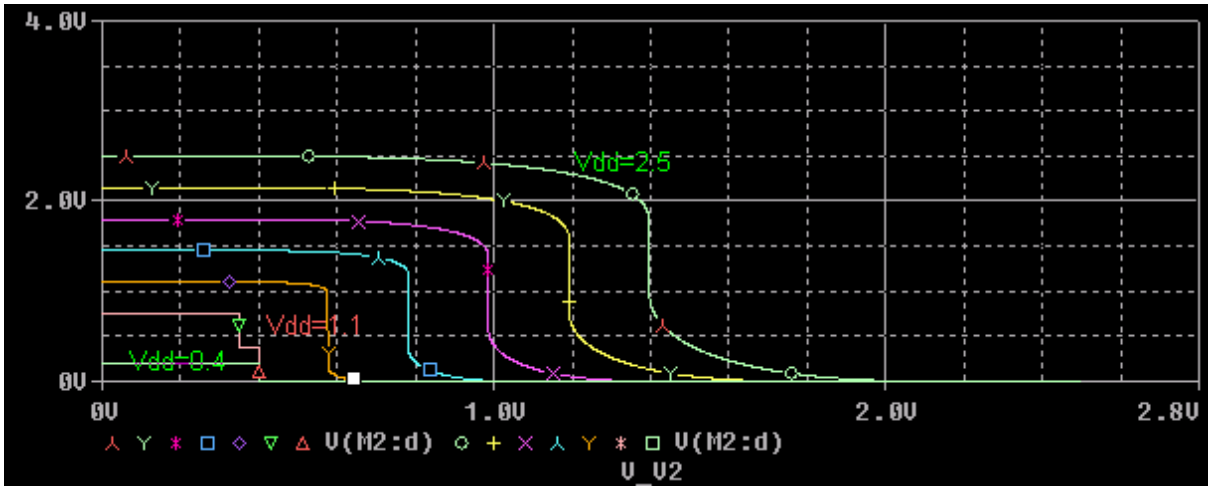
The CMOS inverter is quiet robust. Vm stays relitively constant over the change. In the tests we increased Wp/Wn ratio by 16 fold. The Vm only increased by little over 0.5 Volts.

D) How to change the switching threshold to get a correct output response.

If the Zero value is noisy then we must raise the switching threshold, to do this we would make tihe Pmos wider, or the NMOS narrower.
If the One voltage is noise then some times the Ones might look l;ike zeros, unless we lower the switching voltage.

Noisy Zero (1.4V) (Vin Green, Vout Red)	**Noisy One (1.2V)** (Vin Green, Vout Red)
Without Correction (Wp/Wn=2) 	Without Correction (Wp/Wn=2) 
With Correction (Wp/Wn=8) 	With Correction (Wp/Wn=1/4) 

E) Investigate how scaling V_{DD} affects the Voltage Transfer Curve (VTC) of the inverter



We can see that as Vdd decreases:

- The curve moves to the left, so Vm decreases.
- The slope becomes steeper thus difference between V_{IL} and V_{IH} decreases.
- The curve becomes smaller – lower output and input voltages can be used.

F) Find Wp/Wn ratio for Symmetric Propagation Delay

Though experimentation I found that a ratio of Wp/Wn=1.13/1 achieved a symmetric $t_{pLH}=t_{pHL}$=6.94ns.

This is because the resistance is , $R \propto \frac{1}{\left(\mu C_{ox}\left(\frac{W}{L}\right)\right)}$ where μ is the carrier mobility.

The mobility of holes is much lower than that of elections. Thus to counter act it – to make its resistance the same as for a NMOS, we must increase its (relative) width.

The lecture notes suggest that $\mu_n=500\ \mu_p=180$, which would actually suggest a that Wp/Wn ratio should be much higher than what I found. However increasing the width also increases the parasitic capacitances which increases the time.

G investigate relationship between Wp/Wn and Propagation Delays

Wp (um)	Wn (um)	T_{LpH} (ns)	T_{pHL}(ns)	Tp	Wn+Wp (um)
4	1	2	6.95	4.48	5
3.5	1	2.33	6.92	4.63	4.5
3	1	2.71	6.91	4.81	4
2.5	1	3.38	6.93	5.16	3.5
2	1	4	6.95	5.47	3
1.5	1	5.5	6.92	6.21	2.5
1	1	7.63	6.95	7.29	2
1	1.5	7.5	5.04	6.27	2.5
1	2	7.48	3.47	5.48	3
1	2.5	7.48	2.89	5.18	3.5
1	3	7.49	2.52	5.01	4
1	3.5	7.48	2.17	4.82	4.5
1	4	7.48	1.78	4.63	5

We see that, the rise time is roughly proportional to Wp (though it is also proportional to a lesser degree on the 1/Wn). The converse is to for the fall time.
We see that the average propagation delay is proportional to the sum of the widths.

H investigate relationship between Vdd and Propagation Delays

Note: in this experiement, unlike in E, I have explictly limmited the Gate voltage to be less than/equal to VDD.

Vdd (volts)	T_{LpH} (ns)	T_{pHL}(ns)	Tp (ns)	
	0.4	2859.14	<Evaluation Failed>	
	0.58	159.88	185.38	172.63
	0.75	56.63	65.18	60.9
	0.93	32.25	37.03	34.64
	1.1	24.61	25.59	25.1
	1.28	17.96	19.88	18.92
	1.45	14.42	16.35	15.39
	1.63	12.14	12.74	12.44
	1.8	11.11	11.26	11.19
	1.98	9.51	10.13	9.82
	2.15	8.34	9.26	8.8
	2.33	6.99	8.21	7.6
	2.5	6.99	6.95	6.97

As expected, when Vdd=0.4, which is equal in magnitude to the Vt of the transistors, the inverter fails to function.
For the other results we see that Tp is inversely proportional to the Vdd. It falls off in the expected shape for a reciprocol relationship. At voltages furthur from the point in which symetric response was calculated (2.5) the propergation delays are less symetrical.

I) Various Inverters

A) Traditional Inverter

This is the traditional design for an inverter that has been simulated thoughout all earlier questions in this lab.

Advatages:

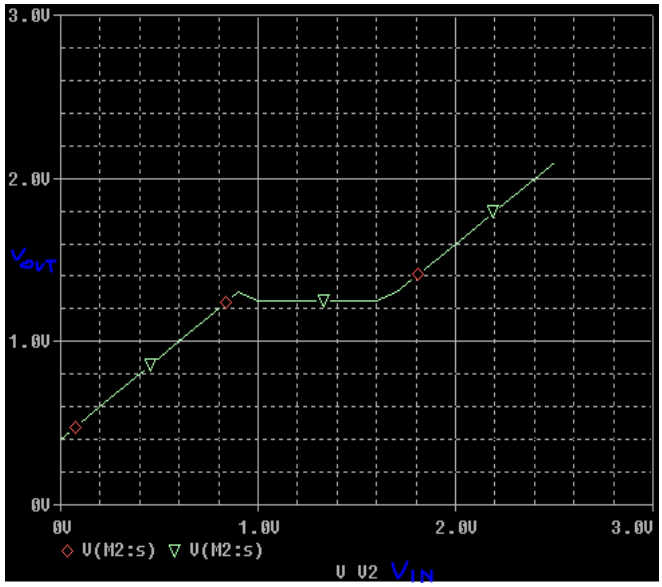
- Actually works as a inverter.
- Full output swing
- No static power disipation

Disadvantages:

- Uses a PMOS, which is expensive.

B) Upside down “inverter” (Buffer)

Vin	Inital Vout	NMOS State	PMOS State	Final Vout
High (2.5v)	Low	On	Off	High (2.1v)
High (2.5v)	High	Off	Off	High
Low (0v)	High	Off	On	Low (0.4v)
Low (0v)	Low	Off	Off	Low



Roughly this device is a buffer. The output is the same as the input (but weaker).

Advantages

- No static power disipation
- Uses only 2 transistors, vs the 4 required for the double inverter buffer

Disadvantages

- Not a inverter
- Doesn't have full output swing

C) PMOS only "inverter"

Send a High, and output is floating. When floating the output will start at what is was before but slowly (due to leakage) fall.

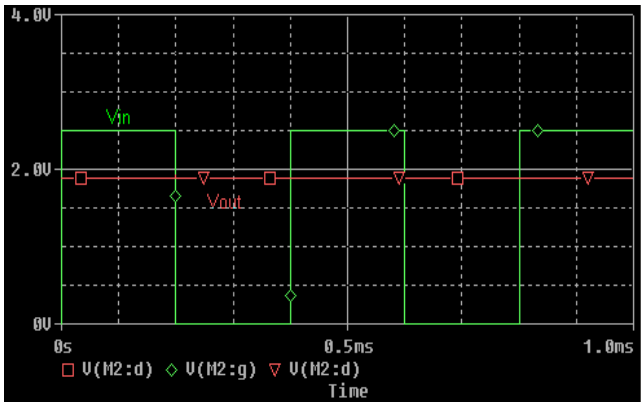
Send a Low, and output is connected to a short circuit between Vdd and Ground – both transistors are on, so it acts as a voltage devider.

However as the top Vbs is nonzero so, it is affected by body effect. This increases its Vt, increasing its apparent resistance (nonlinearly), when using the switch resistor model[1].

So $R_{bottom}>R_{top}$:

$$V_{out}=V_{dd}\frac{R_{bottom}}{\left(R_{bottom}+R_{top}\right)}>\frac{V_{dd}}{2}=1.25\text{v}$$

Vin	Top PMOS State	Bottom PMOS State	Vout
High (2.5v)	Off	Off	Floating
Low (0v)	On	On	>1.25v Actual: 1.89V



Advantages

- None – not useful

Disadvantages

- Static Power Disipation if input low
- Doesn't act as a inverter

1 Switch resistor model doesn't really work when considering body effect. This is quiet hand wavy.

D) NMOS only "inverter"

Send a Low, and output floating. When floating the output will start the same as before but slowly (due to leakage) fall.

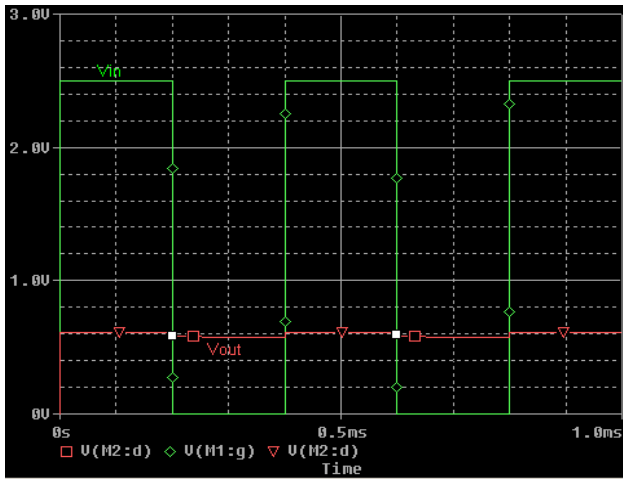
Send a High, and output is connected to a short circuit between Vdd and Ground – both transistors are on, so it acts as a voltage devider.

However the top NMOS V_{BS} is nonzero so, it is affected by body effect. This increases its Vt, and has a nonlinear effect, increasing its apparent resistance, when using the switch resistor model[2].

So $R_{top}>R_{bottom}$:

$$V_{out}=V_{dd}\frac{R_{bottom}}{\left(R_{bottom}+R_{top}\right)}<\frac{V_{dd}}{2}=1.25\text{v}$$

Vin	Top NMOS State	Bottom NMOS State	Vout
High (2.5v)	On	On	<1.25v Actual: 0.615V
Low (0v)	Off	Off	Floating



Advantages

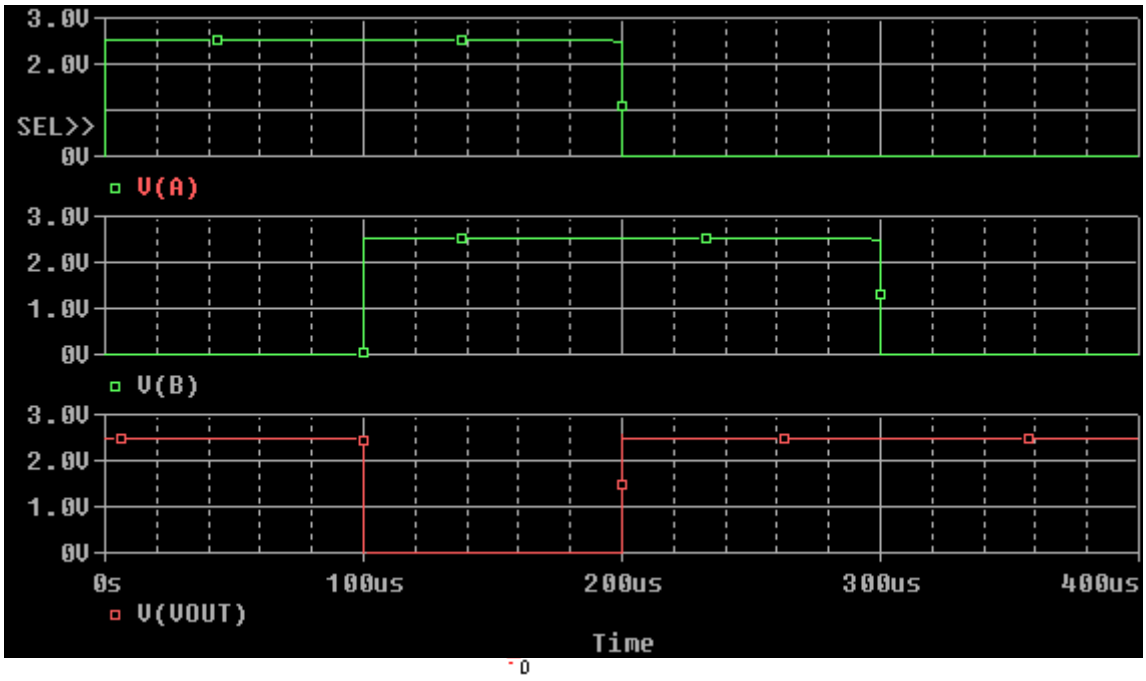
- None – not useful

Disadvantages

- Static Power Disipation if input High
- Doesn't act as a inverter

2 Switch resistor model doesn't really work when considering body effect. This is quiet hand wavy.

J) NAND gate

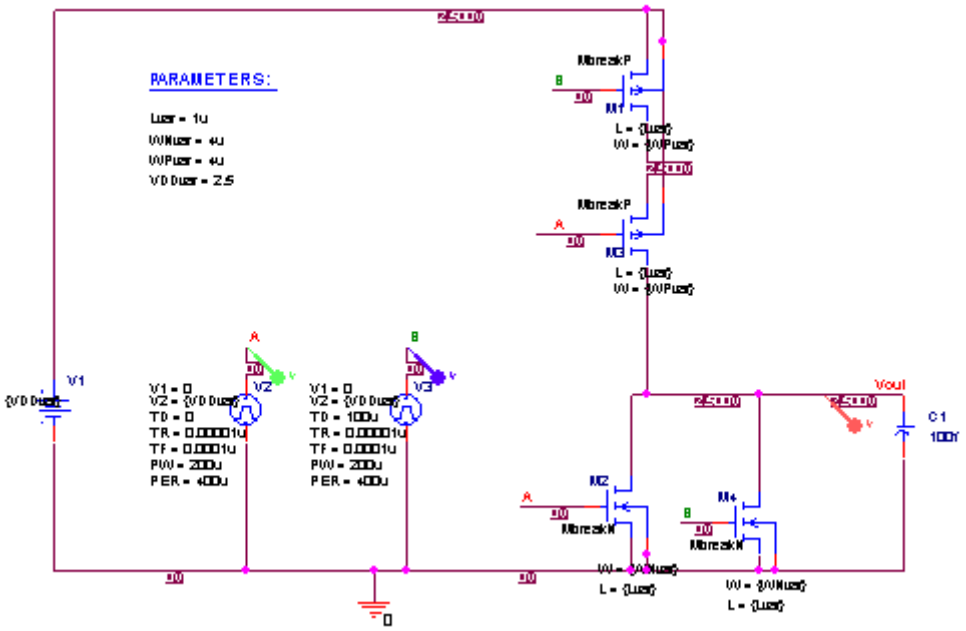


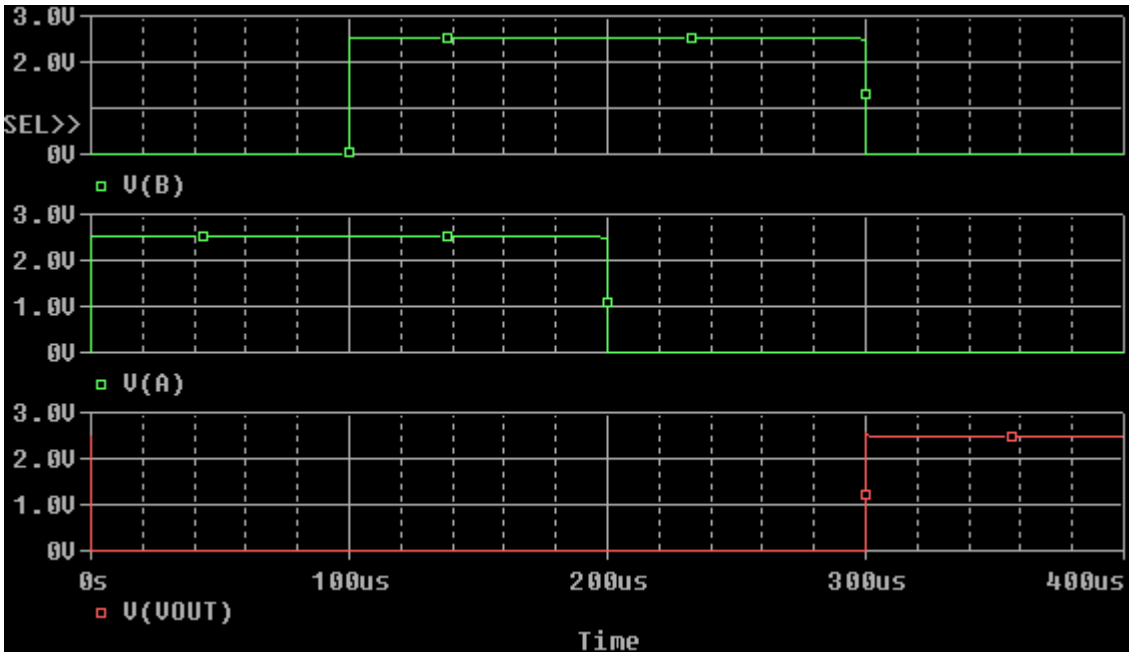
Worst Case Fall time is AB=00, Tp_{HL}=3.58ns.

Worst Case Rise Time is AB=10., tp_{LH}=2.08ns

This is slightly lower that AB=01 , which has a rise time of 1.75ns, this is due to capacitance between the 2 NMOSes.

K) NOR gate





Worst Case Rise Time is AB=11., tp_{LH}=4.1ns

As expected this is longer that the worst case rise time for the NAND gate above because of the lower mobility of PMIOS

Worst Case Fall time is AB=01, Tp_{HL}=1.78ns.

This is slightly lower that AB=10 , which has a fall time of 1.74ns, this is due to capacitance between the 2 PMOSes.